

**ABSTRACT**

A system and software for improving the performance of processors by incorporating an execution unit operable to decode and execute single instructions in an instruction set comprising

- 5 (a) group instructions that operate on a plurality of data elements in partitioned fields of a register to produce a catenated result, (b) aligned memory operations that move data between memory and register where the memory operand is aligned, and (c) unaligned memory operations where the memory operand is unaligned.